A 0.5-20GHz Quadrature Downconverter

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***Abstract* — A quadrature downconverter with 4GHz IF bandwidth and working over the 0.5-20GHz RF frequency range has been designed, fabricated, and tested. The downconverter uses a frequency doubling and dividing scheme to generate quadrature local oscillator signals from 0.5-17GHz and a pair of Gilbert-cell mixers to perform downconversion. When the IF outputs are combined with a commercial quadrature hybrid, the mixer achieves an image rejection ratio greater than 35dB over the entire band with no on-chip calibration or tuning. The active die area is approximately 0.5x1mm^2.**

***Index Terms* — Quadrature downconverter, frequency doubler, frequency divider, IQ mixer, image rejection, wideband, broadband, receiver.**

I. Introduction

With the arrival of robust monolithic semiconductor processes offering transistors with cutoff frequencies in the low hundreds of GHz, the cost of analog processing has dropped enormously, thereby making an economic argument for integrating analog circuit blocks. For applications such as radio astronomy, electronic surveillance, broadband communications, and microwave instrumentation, a wideband quadrature downconverter is a useful building block. While there has been considerable work in recent years towards demonstrating the feasibility of integrated receivers with moderate bandwidth for uses such as software-defined and cognitive radio [1]-[3], to the authors' knowledge, no circuits have been reported that can be tuned all the way from 0.5GHz to 20GHz. Thus, there is no turnkey solution for those looking to build inexpensive systems covering this large of a fractional bandwidth. The aim of this work is to provide a solution to this problem.

One example of an application in which wideband quadrature downconverters would be helpful is with inexpensive radio astronomy receivers. A block diagram of the simplest possible system that might be used in a radio astronomy array appears in Fig. 1(a). In this single polarization system, a common local oscillator (LO) is distributed to a number of receivers, each of which is connected to a broadband antenna (or feed). The output of each antenna is directly coupled to an LNA which, depending upon the application, may or may not be cooled. After the noise performance of the receiver has been set by the LNA, the RF band of interest is sampled using a quadrature downconverter, with LO frequency set at the center of the RF band. The downconverted in-phase (I) and quadrature (Q) components are then fed through anti-aliasing filters and digitized using GHz bandwidth converters. Finally, the digital outputs of each channel are fed to a central processor where correlation, beam forming, or other array processing is performed.

This paper begins with a discussion of the design of a 0.5-20GHz quadrature down-converter. Particular interest will be paid to the challenges that come with trying to achieve quadrature over a 36:1 bandwidth. Next, measured results of the mixer will be given. Finally, the paper will conclude with a brief discussion of possible future enhancements to the design.

II. Design

While mixers are intrinsically broadband components, generating an accurate quadrature LO signal on-chip over a very large frequency range is not trivial. Thus, a first step in the design of a quadrature downconverter is to select a topology for generating the quadrature LO. Components commonly used to achieve this task include quadrature hybrid couplers, polyphase filters, quadrature oscillators, and frequency dividers. Choice of topology involves consideration of both the required LO phase accuracy and the bandwidth over which accurate quadrature must be generated. The required accuracy in the phase of the LO depends upon the desired image rejection ratio (IRR). To achieve an IRR of greater than 40dB, it is necessary that the LO quadrature be accurate to within 1°. For this work, the frequency divider method is used. This topology was chosen for its simplicity, small die area, and intrinsic broadband nature.

A block diagram of the proposed downconverter appears in Fig. 1(b). The circuit consists of a pair of

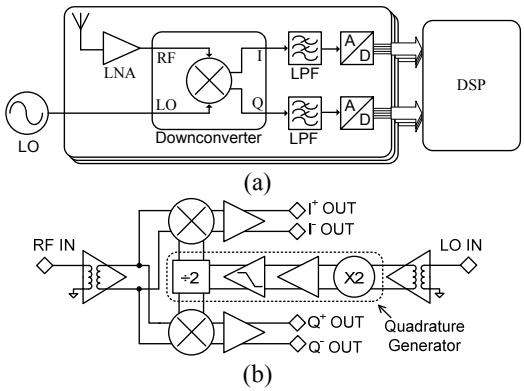

Fig. 1: (a) Example system requiring a broadband downconverter. (b) Block diagram of proposed IC.

mixers whose LO ports are driven from the outputs of an on-chip quadrature generator. Active baluns have been included on chip in order to avoid needing differential signals coupled into the chip. Each active balun consists of a differential Cherry Hooper amplifier (see [4]) with each of its two inputs driven by emitter follower buffers to allow for a dc coupled input.

The mixers are Gilbert cells, and are each loaded with a differential capacitance designed to introduce a pole in the IF response near 4GHz. At the output of each mixer is an IF buffer amplifier intended to drive 100Ω differentially. One port of each IF amplifier can be terminated in 50Ω at the expense of 6dB in conversion gain. The remainder of this section is devoted to discussion of the quadrature generator.

It is a well known fact that a digital divider can provide quadrature signals at one half of its clock frequency. From a system design point of view, it is far more practical to couple a LO signal into the chip at the fundamental frequency, 0.5-18GHz, rather than at the second harmonic. Adopting this approach requires generating the second harmonic of the LO on chip using a frequency doubler circuit.

Before discussing the details of the circuitry, it will be useful to review the tradeoffs in broadband current-mode digital divider design. At the low frequency end, the divider is limited by its hold time, or how long the latching circuit can maintain its state while its inputs are in the indeterminate state. This means that clock signals with fast rise time are needed to minimize the requirement on hold time. At high frequencies, the divider is response limited; that is, the charging time constants at the latching nodes approach the period of the clock [5]. This can be overcome to a certain extent by increasing the amplitude of the clock signal, in turn decreasing the charging time constants. However, at some point, the circuit simply cannot respond fast enough and the divider ceases to operate.

When using a digital divider to generate quadrature signals, it is also necessary that the clock signal have 50% duty cycle. The reason for this is that its positive and negative edges are each used to clock one of the latches in the divider and it is therefore necessary that these edges are separated by exactly a half cycle for ideal operation. Any deviation from 50% duty cycle translates directly into the phase balance of the local oscillator; that is a 1% error in duty cycle will translate into a 3.6° phase error.

In summary, the divider requires large clock signals at the high frequency end, where operation requires reducing the charging time constants, and square wave inputs at the low frequency end where the amount of time in undetermined clock states needs to be minimized. In addition, for accurate quadrature generation, the clocking signal must have as close to 50% duty cycle as possible.

As frequency divider operation requires 50% duty cycle, the frequency doubler must operate with output frequencies in the 1-36GHz range and low even-order distortion. To meet the bandwidth constraint, a Gilbert cell mixer can be used as a frequency doubler by providing a common LO and RF signal. As the frequency doubler must operate over a 36:1 range, it is not possible to include the filtering necessary to remove even order harmonics generated in the process of multiplying the input sine wave with the LO switching waveform and degradation of the output signal duty cycle will occur unless the mixer is operated with both its RF and LO ports driven in the small-signal domain. This leads to conversion loss proportional to the input amplitude squared, rather than the linear relationship that is typical of mixers driven in saturation. Furthermore, when it is operated in this manner, it is difficult to obtain large output swings. Thus, there is a tradeoff between the output swing of the frequency doubler and its duty cycle.

To relax this tradeoff, a broadband gain block can be introduced between the frequency doubler and the digital divider. This gain block allows the doubler to be driven with smaller input signals and also attenuates harmonic content occurring above its maximum frequency of operation. To extend the minimum operating frequency of the divider to a lower value, a

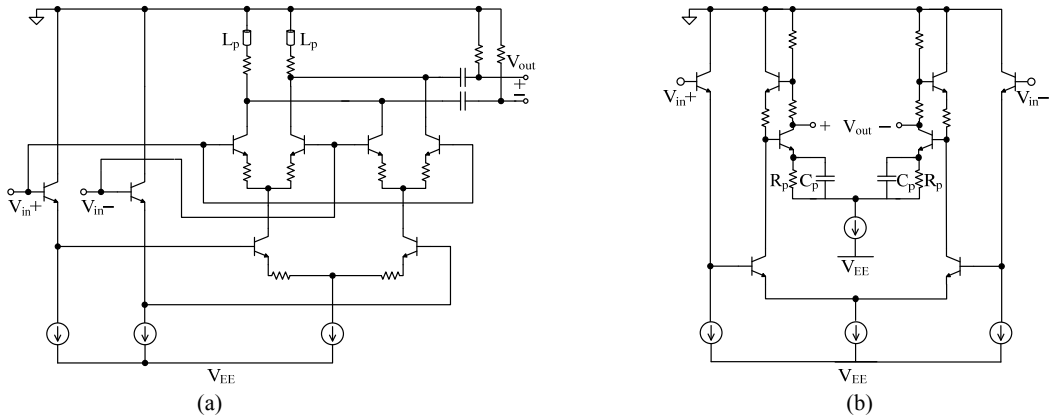

Fig 2: Simplified schematics of some of the main circuit blocks. (a) Frequency doubler and (b) cascadable gain block.

clipping amplifier, which has high gain at low frequencies, near unity gain at the upper frequency of operation, and high slew rate can be included as the final stage before the divider. Inclusion of both a broadband gain stage and a clipping amplifier after the frequency doubler allows the signal clocking the divider to have 50% duty cycle, sharp edges at low frequency, and adequate drive over the entire band.

The final circuit consists of a Gilbert cell based 0.5-18GHz frequency doubler, a 36GHz 20dB gain block, a clipping amplifier, and a 1-36GHz input frequency divider. A simplified schematic diagram of the frequency doubler appears in Fig 2(a). The frequency doubler consists of a gilbert cell mixer having both its RF and LO ports driven by the same input signal. To extend the bandwidth of the doubler, peaking inductors, L_p, were introduced in the load. These inductors were implemented using short-circuited shielded transmission lines. In addition, to avoid differential dc offsets from the squaring operation, the output of the doubler is coupled to the broadband amplifier via a 200MHz highpass filter.

The gain block is implemented as a two-stage amplifier with each stage consisting of differential cherry hooper amplifiers as shown in Fig 2(b). To extend the operating bandwidth of the gain stage, peaking elements R_p and C_p are used. As a final note, it should be recognized that, since the IF bandwidth goes out to 4GHz, the circuit can also be used to upconvert signals in the range below 4GHz so long as the output frequency is within the IF bandwidth.

III. Measurements

The downconverter described in section II was implemented in the IBM BICMOS 8HP process. A die photograph appears in Fig. 3. While die area is approximately 1.7x1.5mm^2, the active area is just 1x0.5mm^2. The chip size is dominated by the transmission lines and bondpads required to test the circuit. The circuit draws 350mW from a single –2.5V supply. While the power dissipation could be reduced, it is not terribly important for this application. The downconverter was evaluated using on-wafer measurements and no trimming or tuning was used.

The minimum input referred power required to operate the divider is plotted as a function of frequency in Fig. 4. The divider works with input frequencies from 1-34GHz with less than -15dBm of external LO power required to operate the divider over the majority of the band. The conversion gain of the downconverter assuming a differential output appears in Fig. 5 as a function of IF frequency. The mixer has less than 3dB roll-off for IF frequencies up to 4GHz and $\pm$1dB of gain flatness over the entire RF frequency range.

The amplitude and phase balance of the downconverter were measured at an IF frequency of 50MHz using a Tektronix TDS3014B oscilloscope and the

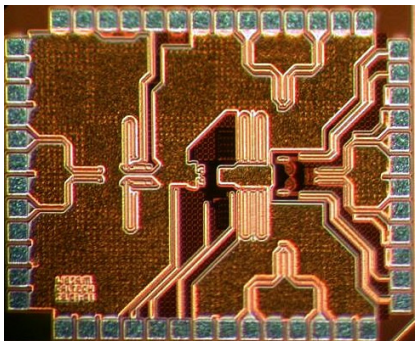

Fig. 3: Die photograph. Chip dimensions are 1.5x1.7mm^2.

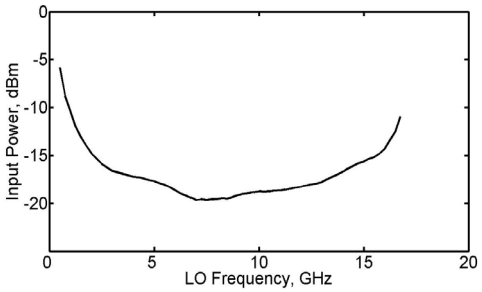

Fig. 4: Measured input power required to operate frequency divider as a function of divider output frequency. Power is referenced to the LO input bondpad.

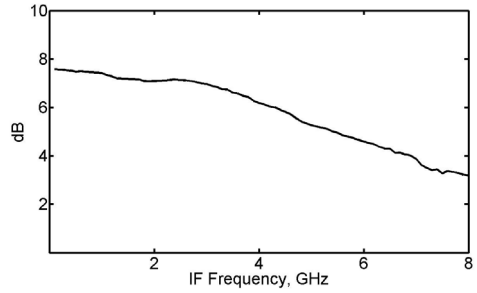

Fig. 5: Measured conversion gain as a function of IF frequency. The RF frequency is 2.05GHz. If one of the differential outputs is terminated, the gain is 6dB lower.

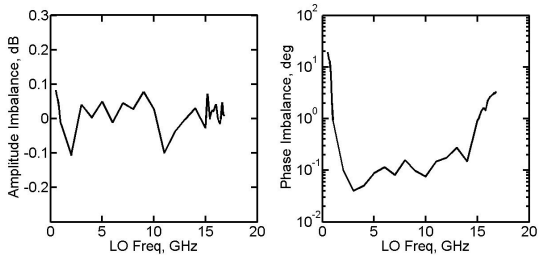

Fig. 6: IF amplitude and phase balance as a function of LO frequency with near optimum LO drive. The IF frequency is 50MHz. When the outputs of the downconverter feed an ideal quadrature hybrid, this balance corresponds to an average image rejection ratio of greater than 47dB for LO frequencies in the range of 1-16GHz.

TABLE I: Mixer performance metrics

RF Freq.	LO Freq.	IF Freq.	IRR	Conv. Gain	Input P1dB	Input IP2	Input IP3	RF-IF Isolation	LO-IF Leakage
GHz	GHz	GHz	dB	dB	dBm	dBm	dBm	dB	dBm
0.5-20	1-16	DC-4	>35	7±1	-11	25	-4	>50	<-55

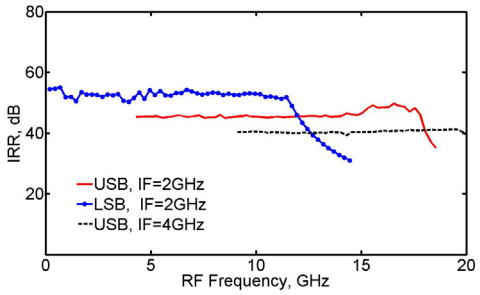

Fig. 7: Measured image rejection versus of RF frequency with near optimum LO drive. The difference between the upper and lower sideband rejection is thought to be due to small differences in the electrical lengths of the IF cables.

results appear in Fig. 6. For LO frequencies from 1-16GHz, the amplitude and phase balance are better than 0.1dB and 2° respectively, corresponding to a worse case image rejection ratio of approximately 35dB when the outputs of the mixer are fed into an ideal quadrature hybrid. The phase balance degrades below 1GHz due to even order distortion generated in the frequency doubler and above 16GHz as the divider approaches its maximum frequency of operation.

A Krytar 1830 2-18GHz quadrature hybrid was used to evaluate the IRR of the downconverter. The IRR is plotted as a function of RF frequency in Fig. 7 and is greater than 40dB over most of the band. At lower frequencies, there is approximately 8dB of disagreement between the 2GHz IF upper and the lower-sideband IRR which is explained by small differences in the electrical lengths of the IF cables. In addition, it can be observed that the IRR is rolling off as the LO frequency approaches 16GHz (the maximum LO frequency for each of the curves) due to the degradation in LO phase error at the high end of the lock range. Additional performance metrics appear in Table I.

IV. Conclusion

The design of a 0.5-20GHz quadrature downconverter suitable for broadband applications has been presented. The amplitude and phase balance have been measured and found to be sufficient to achieve an IRR of greater than 35dB over the entire RF operating range with the LO tuned from 1-16GHz. Using a commercial quadrature hybrid, image rejection ratios of over 40dB have been measured over the majority of the band with IF frequencies of 2 and 4GHz.

There are several ways in which this downconverter can be improved. While the IRR was found to be quite good, the problem of harmonic response has not been addressed. This is important for broadband receiver applications, as harmonics of the LO can mix with strong RFI, corrupting the received data. In a future iteration, one improvement to the design would be to include extra LO phases in order to reject harmonic responses. A three phase scheme capable of rejecting the responses of the third and fifth LO harmonics was presented in [2]. In combination with an on-chip bank of switchable lowpass/highpass filters, it is believed that this scheme can provide sufficient rejection of the harmonic response to meet system requirements. Second order improvements include adding a phase control option to the divider using a method similar to that presented in [6], improving the dynamic range, and reducing power dissipation. Finally, including the anti-aliasing filter along with the analog to digital converter on chip would help to reduce IF mismatch and make the chip more attractive for integration into a large system.

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